

100V N-Channel Power MOSFET

Description

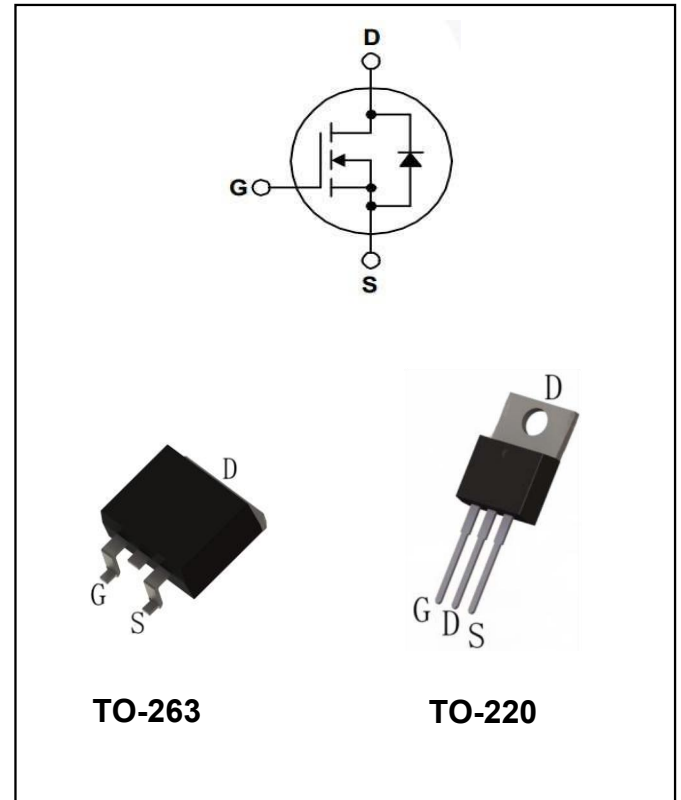
MPT042N10, the N-channel Enhanced Power MOSFETs, is obtained by advanced double trench technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This is suitable device for motor drivers and high speed switching applications.

General Features

- ① $V_{DS}=100V$, $R_{dson}<4.2m\Omega$ @ $V_{GS}=10V$, $I_D=120A$ (Typ: $3.5m\Omega$)
- ② Fast Switching
- ③ Low On-Resistance ($R_{DS(on)}\leq 4.2m\Omega$)
- ④ Low Gate Charge
- ⑤ Low Reverse transfer capacitances
- ⑥ High avalanche ruggedness
- ⑦ RoHS product

Application

- ① Switching application
- ② Motor drivers



Package Marking And Ordering Information:

Ordering Codes	Package	Product Code	Packing
MPT042N10-P	TO-220	MPT042N10P	Tube
MPT042N10-S	TO-263	MPT042N10S	Tape Reel

ABSOLUTE RATINGS at $T_c=25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	100	V
I_D	Continuous Drain Current, Silicon Limited	170	A
	Continuous Drain Current, Package Limited	120	A
	Continuous Drain Current @ $T_c=100^\circ C$, Silicon Limited	107.8	A
I_{DM} ^{Note1}	Pulsed Drain Current	480	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS} ^{Note2}	Avalanche Energy	306	mJ



P _D	Power Dissipation	227.2	W
	Derating Factor above 25°C	1.82	W/°C
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	260	°C

Note1: Repetitive Rating: Pulse width limited by maximum junction temperature Note2: L=0.5mH, I_{as}=35A, Start T_J=25°C

Thermal characteristics

Symbol	Parameter	Max	Units
R _{θJC}	thermal resistance, Junction-Case	0.55	°C/W
R _{θJA}	thermal resistance, Junction-Ambient	62.5	°C/W

Electrical Characteristics at T_c=25°C, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
V _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
		V _{DS} =80V, V _{GS} =0V @T _c =125°C	--	--	100	μA
I _{GSS(F)}	Gate-Source Forward Leakage	V _{GS} =+20V	--	--	100	nA
I _{GSS(R)}	Gate-Source Reverse Leakage	V _{GS} =-20V	--	--	-100	nA
ON Characteristics						
Symbol	Parameter	Test Conditions	Values			Unit s
			Min	Typ	Max	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =50A	--	3.5	4.2	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Pulse width tp≤300μs, δ≤2%						
Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
C _{iss}	Input Capacitance	V _{DS} =50V, V _{GS} =0, f=1MHz	--	7102	--	pF
C _{OSS}	Output Capacitance		--	2584	--	
C _{rSS}	Reverse Transfer Capacitance		--	174	--	
Q _g	Total Gate Charge	V _{DD} =50V, I _D =50A, V _{GS} =10V	--	102	--	nC
Q _{gs}	Gate-Source charge		--	30	--	



Q_{gd}	Gate-Drain charge		--	19.6	--	
Switching Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, I_D=50A,$ $V_{GS}=10V, R_G=3\Omega,$ Resistive Load	--	29	--	ns
t_r	Rise Time		--	33	--	
$t_{d(off)}$	Turn-Off Delay Time		--	48	--	
t_f	Fall Time		--	26	--	
Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
I_S	Continuous Source Current		--	--	120	A
I_{SM}	Maximum Pulsed Current		--	--	480	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V, I_S=50A$	--	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S=50A,$ $di/dt=100A/us$	--	80	--	ns
Q_{rr}	Reverse Recovery Charge		--	189	--	μC



Characteristics Curves

Figure 1. Safe Operating Area

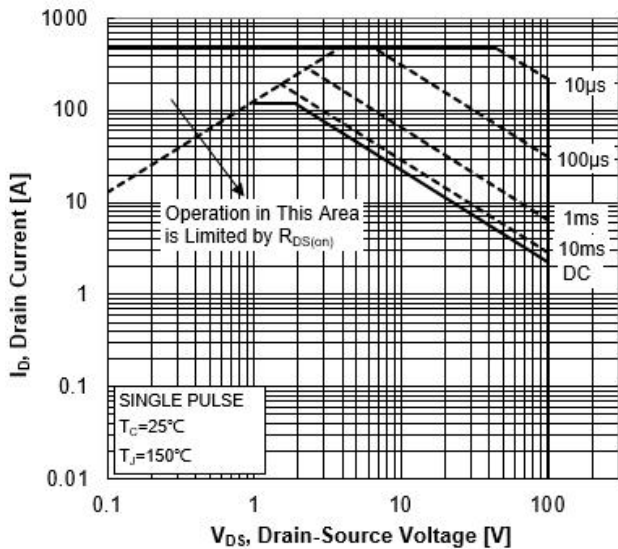


Figure 2. Maximum Power Dissipation vs Case Temperature

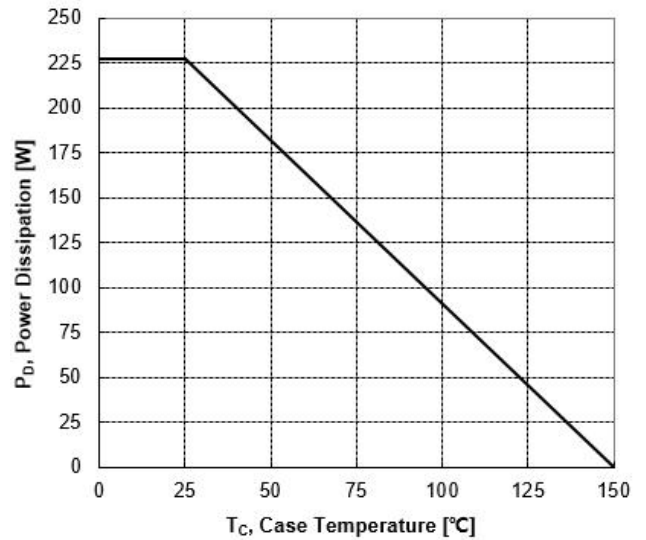


Figure 3. Maximum Continuous Drain Current vs Case Temperature

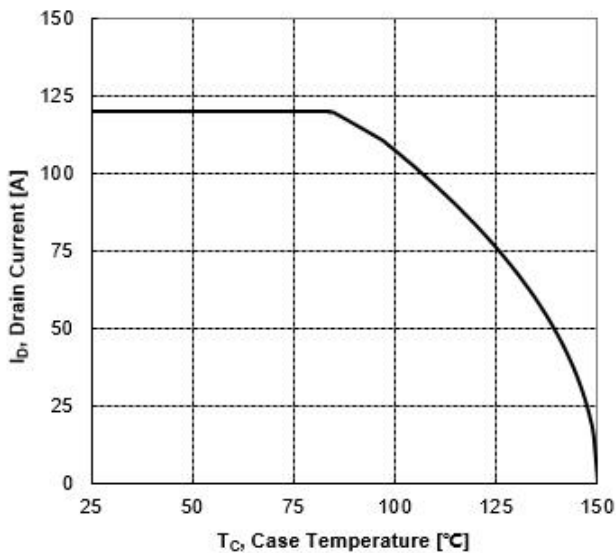


Figure 4. Typical Output Characteristics

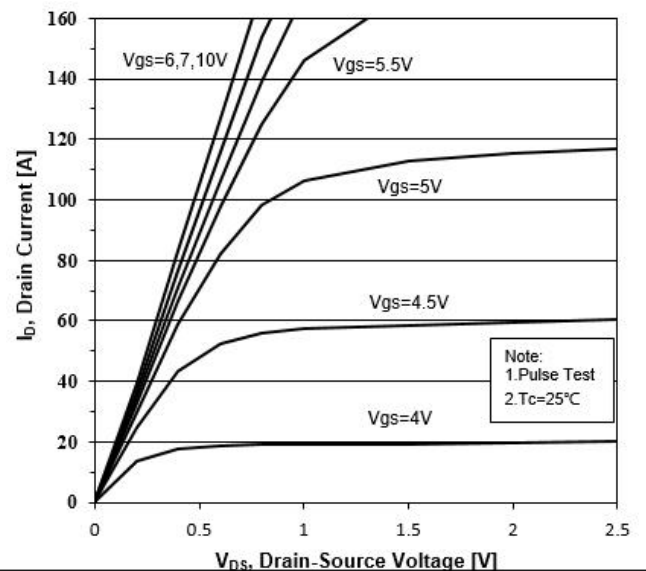


Figure 5. Transient Thermal Impedance

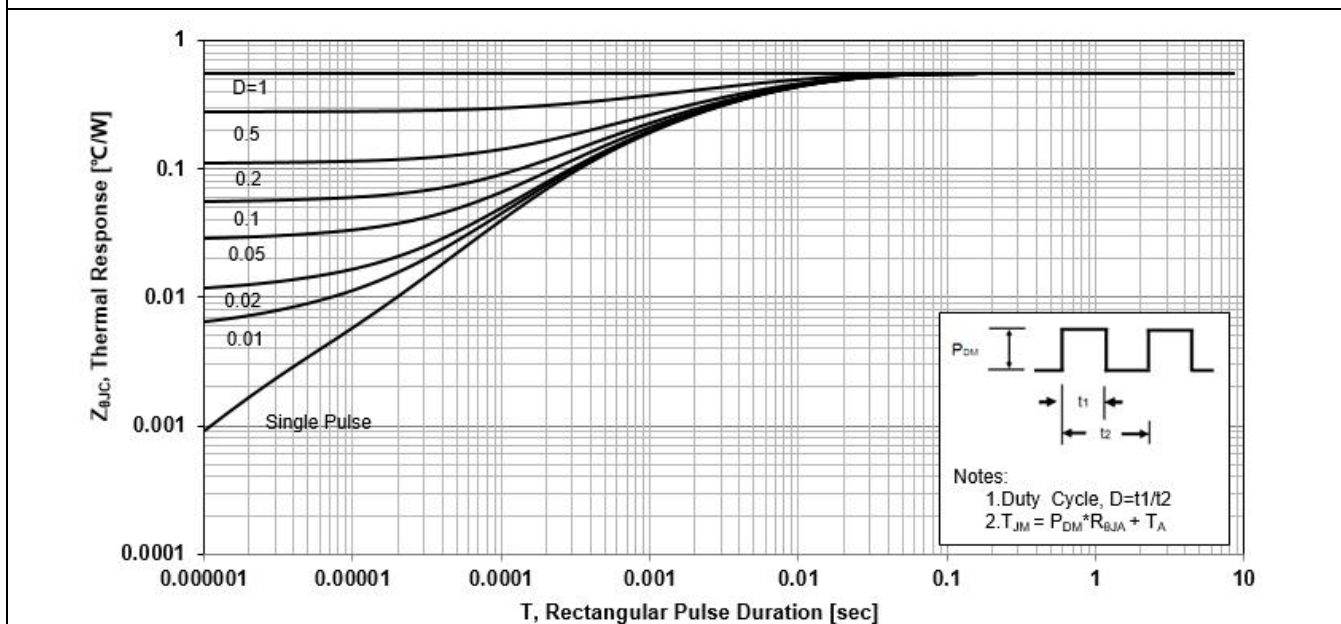


Figure 6. Typical Transfer Characteristics

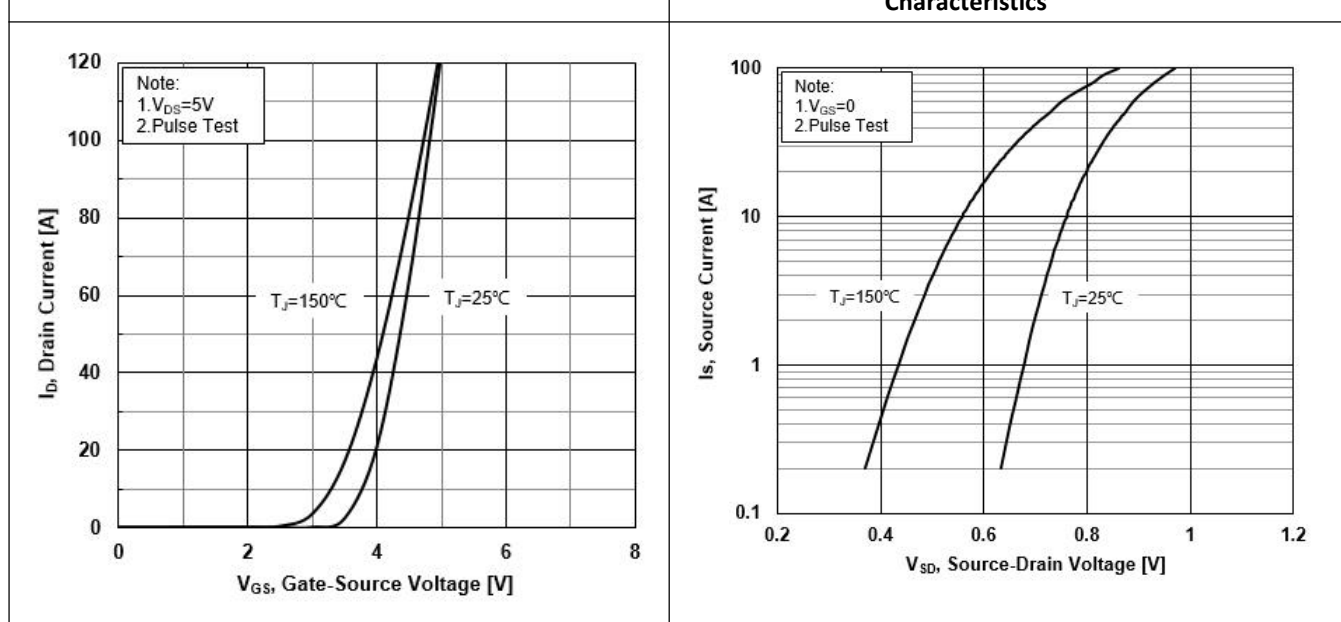


Figure 7. Source-Drain Diode Forward Characteristics

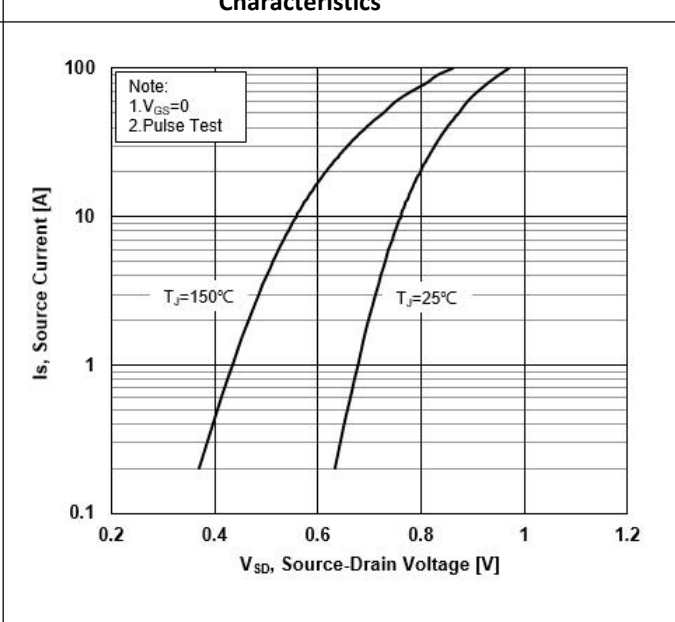


Figure 8. Drain-Source On-Resistance vs Drain Current

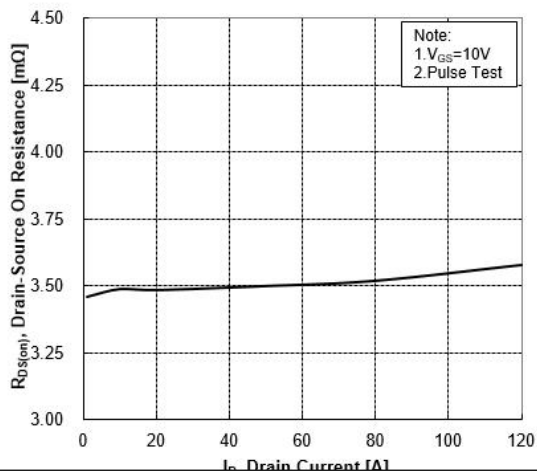


Figure 9. Normalized On-Resistance vs Junction

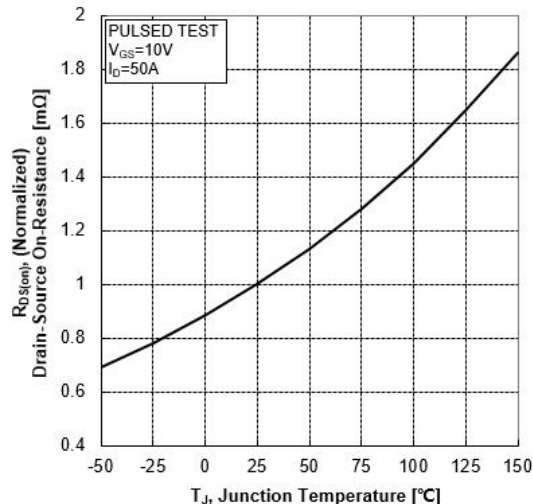


Figure 10. Normalized Threshold Voltage vs Junction Temperature

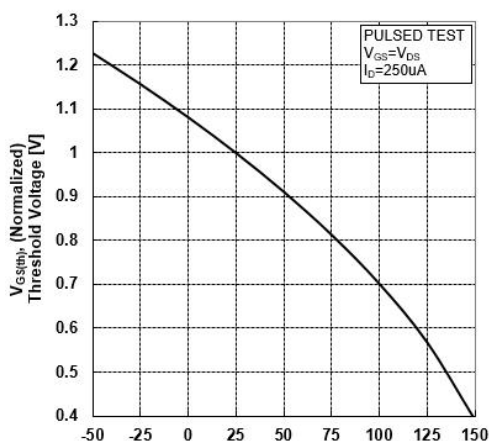


Figure 11. Normalized Breakdown Voltage vs Junction Temperature

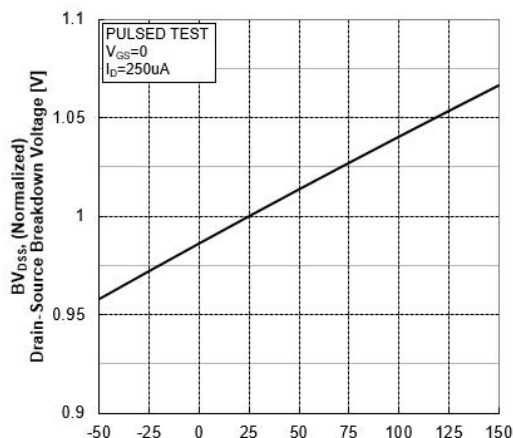


Figure 12. Capacitance Characteristics

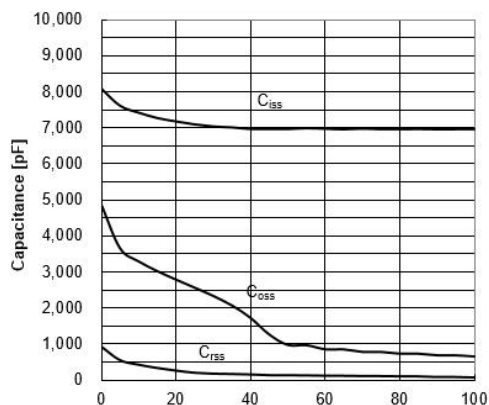
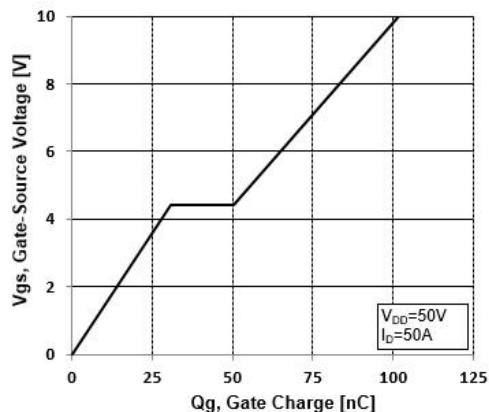


Figure 13. Typical Gate Charge vs Gate-Source Voltage



Test Circuit and Waveform

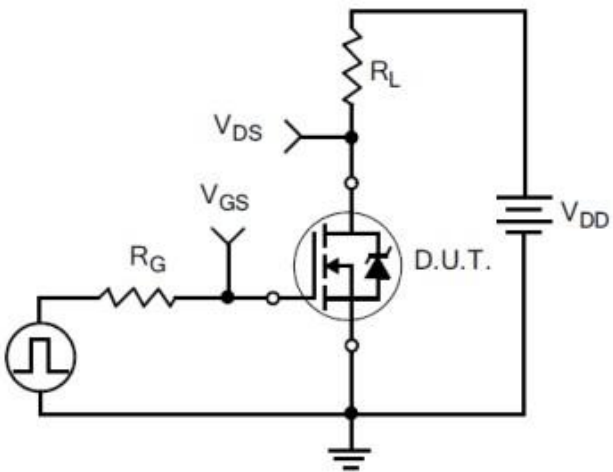
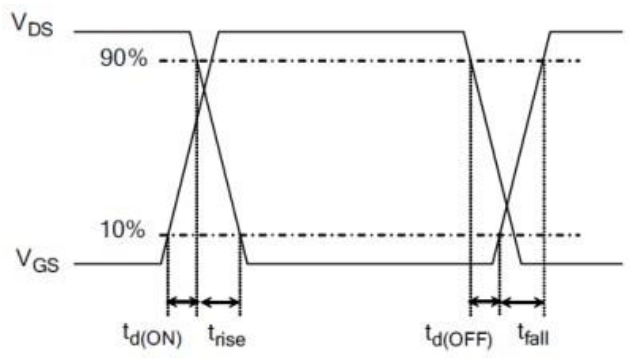
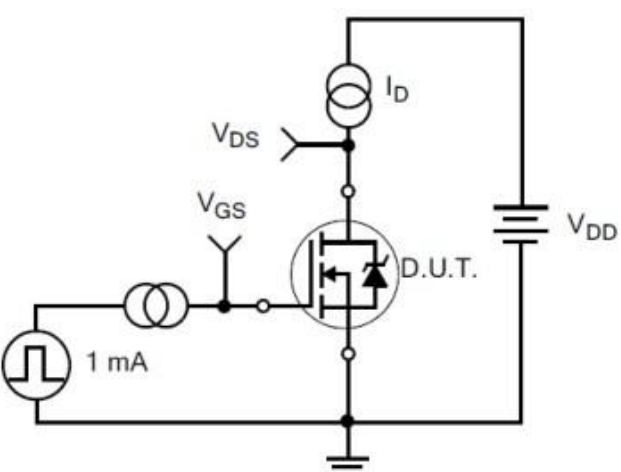
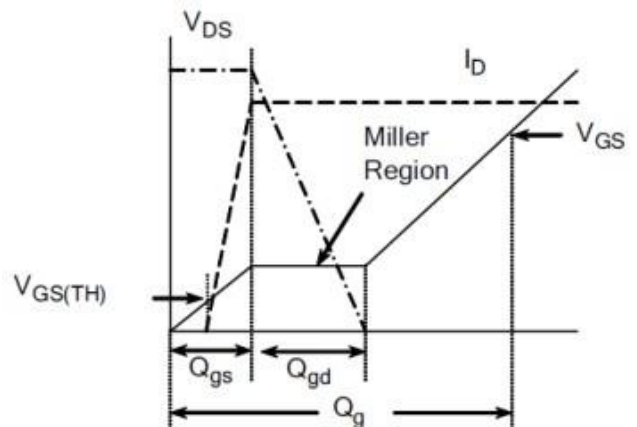
<p>Figure 14. Resistive Switching Test Circuit</p>	<p>Figure 15. Resistive Switching Waveforms</p>
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The gate is driven by a square wave pulse through a gate resistor R_G. The drain is connected to a load resistor R_L and a supply voltage V_{DD}. The drain-source voltage is labeled V_{DS} and the gate-source voltage is labeled V_{GS}.</p>	 <p>The diagram shows the waveforms for V_{DS} and V_{GS} during a switching event. V_{GS} is a square wave pulse. V_{DS} shows a transition from a high state to a low state and back. Key timing parameters are marked: $t_{d(ON)}$ (delay to turn on), t_{rise} (rise time), $t_{d(OFF)}$ (delay to turn off), and t_{fall} (fall time). The 90% and 10% voltage levels are indicated for the transitions.</p>
<p>Figure 16. Gate Charge Test Circuit</p>	<p>Figure 17. Gate Charge Waveforms</p>
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The gate is driven by a square wave pulse through a gate resistor R_G. The drain is connected to a load resistor R_L and a supply voltage V_{DD}. The drain current is labeled I_D and the gate-source voltage is labeled V_{GS}. A 1 mA current source is connected to the gate.</p>	 <p>The diagram shows the waveforms for V_{DS} and I_D during a switching event. V_{GS} is a square wave pulse. V_{DS} shows a transition from a high state to a low state and back. The Miller Region is indicated. Key parameters are marked: $V_{GS(TH)}$ (threshold voltage), Q_{gs} (gate-source charge), Q_{gd} (gate-drain charge), and Q_g (total gate charge).</p>

Figure 18. Diode Reverse Recovery Test Circuit

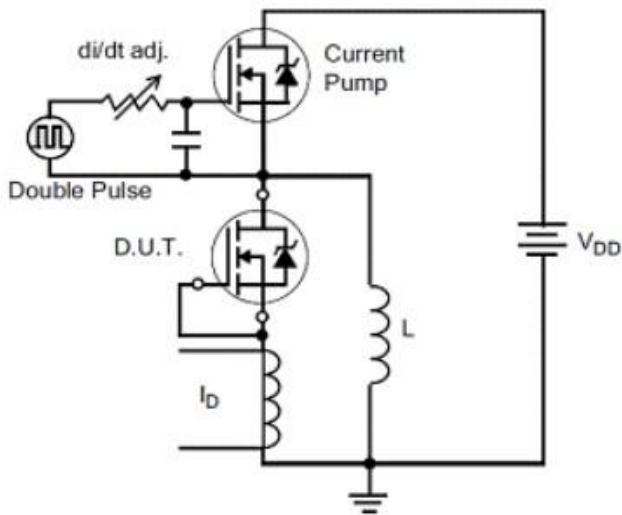


Figure 19. Diode Reverse Recovery Waveform

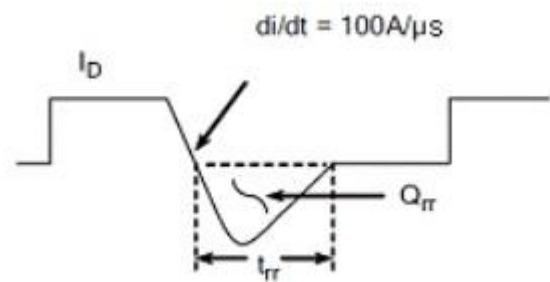


Figure 20. Unclamped Inductive Switching Test Circuit

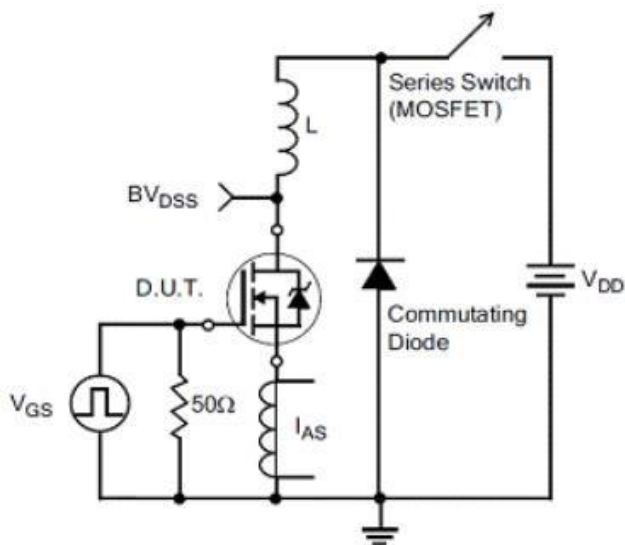
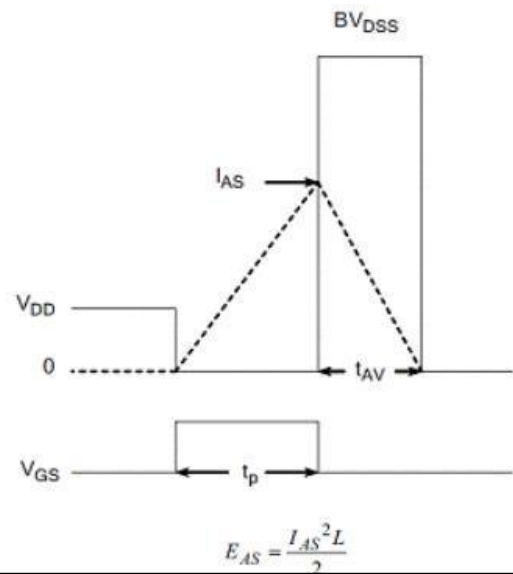
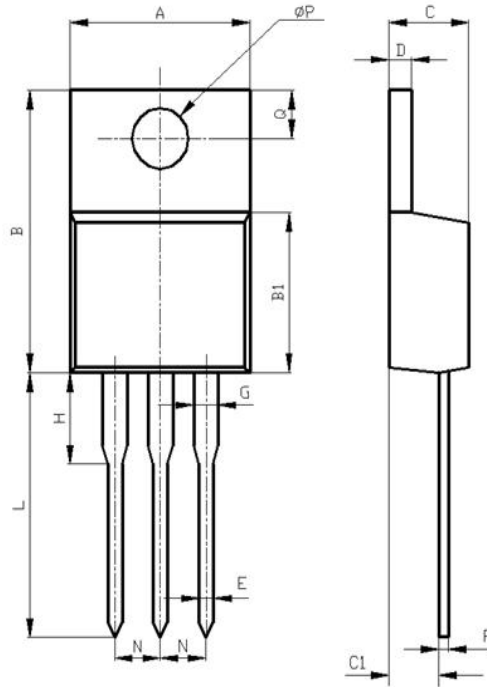


Figure 21. Unclamped Inductive Switching Waveform

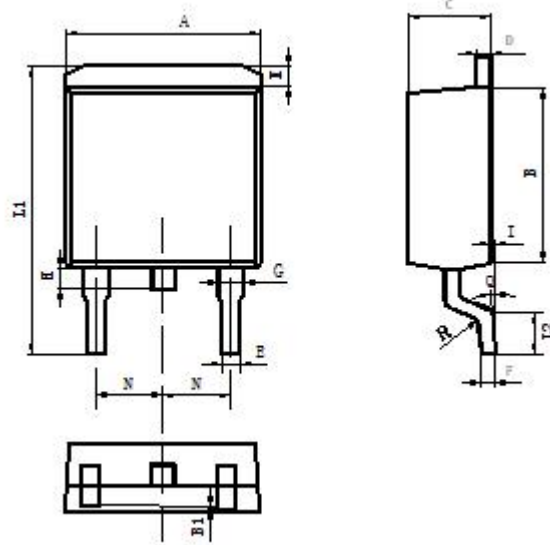


Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ϕP	3.50	3.90

TO-220 Package



Items	Values(mm)	
	MIN	MAX
A	9.80	10.40
B	8.90	9.50
B1	0	0.10
C	4.40	4.80
D	1.16	1.37
E	0.70	0.95
F	0.30	0.60
G	1.07	1.47
H	1.30	1.80
K	0.95	1.37
L1	14.50	16.50
L2	1.60	2.30
I	0	0.2
Q	0°	8°
R	0.4	
N	2.39	2.69

TO-263 Package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

CONTACT:

深圳市迈诺斯科技有限公司（总部）

地址：深圳市福田区华富街道田面社区深南中路4026号田面城市大厦22B-22C

邮编：518025

电话：0755-83273777