

Dual D-Type Flip-Flop with Preset and Clear

74VHC74

General Description

The VHC74 is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D input is transferred to the Q output during the positive going transition of the CK pulse. $\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the CK and are accomplished by setting the appropriate input LOW.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: $f_{\text{MAX}} = 170 \text{ MHz}$ (Typ.) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Power Down Protection is Provided on All Inputs
- Low Power Dissipation: $I_{\text{CC}} = 2 \mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- Pin and Function Compatible with 74HC74
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Logic Symbol

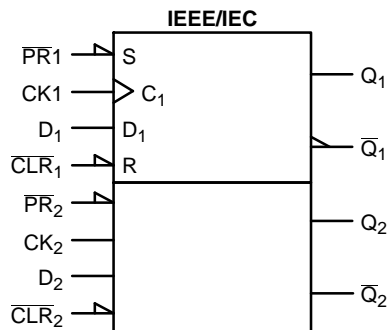
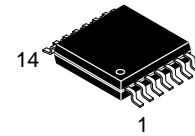


Figure 1. Logic Symbol

TRUTH TABLE

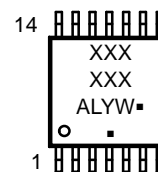
Inputs				Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H (Note 1)	H (Note 1)	
H	H	L	\nearrow	L	H	
H	H	H	\nearrow	H	L	
H	H	X	\searrow	Q_n	$\overline{\text{Q}}_n$	No Change

1. This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) state.



TSSOP-14 WB
CASE 948G

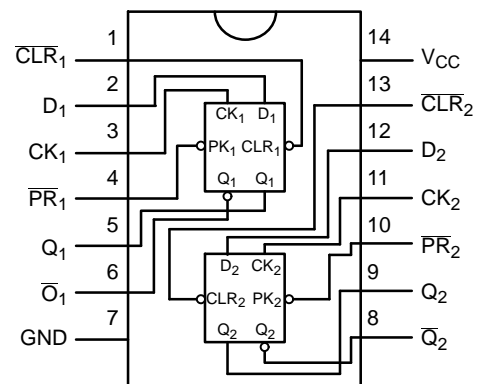
MARKING DIAGRAM



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{\text{CLR}}_1, \overline{\text{CLR}}_2$	Direct Clear Inputs
$\overline{\text{PR}}_1, \overline{\text{PR}}_2$	Direct Preset Inputs
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Output

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

74VHC74

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to +6.5	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, Per Pin	± 20	mA
I_{OUT}	DC Output Current, Per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
I_{IK}	Input Clamp Current	-20	mA
I_{OK}	Output Clamp Current	± 20	mA
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 s	260	$^{\circ}C$
T_J	Junction Temperature Under Bias	+150	$^{\circ}C$
θ_{JA}	Thermal Resistance (Note 2)	150	$^{\circ}C/W$
P_D	Power Dissipation in Still Air at 25 $^{\circ}C$	833	mW
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	>2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{IN}	DC Input Voltage (Note 4)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	$^{\circ}C$
t_r, t_f	Input Rise or Fall Rate $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

74VHC74

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			T _A = -40°C to +85°C		Unit	
				Min	Typ	Max	Min	Max		
V _{IH}	HIGH Level Input Voltage	2.0		1.50	-	-	1.50	-	V	
		3.0-5.5		0.7 x V _{CC}	-	-	0.7 x V _{CC}	-		
V _{IL}	LOW Level Input Voltage	2.0		-	-	0.50	-	0.50	V	
		3.0-5.5		-	-	0.3 x V _{CC}	-	0.3 x V _{CC}		
V _{OH}	HIGH Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.9	2.0	-	1.9	-	V
		3.0			2.9	3.0	-	2.9	-	
		4.5			4.4	4.5	-	4.4	-	
		3.0			2.58	-	-	2.48	-	
		4.5			3.94	-	-	3.80	-	
V _{OL}	LOW Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	-	0.0	0.1	-	0.1	V
		3.0			-	0.0	0.1	-	0.1	
		4.5			-	0.0	0.1	-	0.1	
		3.0			-	-	0.36	-	0.44	
		4.5			-	-	0.36	-	0.44	
I _{IN}	Input Leakage Current	0-5.5	V _{IN} = 5.5 V or GND	-	-	±0.1	-	±1.0	μA	
I _{CC}	Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND	-	-	2.0	-	20.0	μA	

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	3.3 ±0.3	C _L = 15 pF	80	125	-	70	-	MHz
			C _L = 50 pF	50	75	-	45	-	
		5.0 ±0.5	C _L = 15 pF	130	170	-	110	-	
			C _L = 50 pF	90	115	-	75	-	
t _{PLH} , t _{PHL}	Propagation Delay Time (CK-Q, Q̄)	3.3 ±0.3	C _L = 15 pF	-	6.7	11.9	1.0	14.0	ns
			C _L = 50 pF	-	9.2	15.4	1.0	17.5	
		5.0 ±0.5	C _L = 15 pF	-	4.6	7.3	1.0	8.5	
			C _L = 50 pF	-	6.1	9.3	1.0	10.5	
t _{PLH} , t _{PHL}	Propagation Delay Time (CLR, PR-Q, Q)	3.3 ±0.3	C _L = 15 pF	-	7.6	12.3	1.0	14.5	ns
			C _L = 50 pF	-	10.1	15.8	1.0	18.0	
		5.0 ±0.5	C _L = 15 pF	-	4.8	7.7	1.0	9.0	
			C _L = 50 pF	-	6.3	9.7	1.0	11.0	
C _{IN}	Input Capacitance		V _{CC} = Open	-	4	10	-	10	pF
C _{PD}	Power Dissipation Capacitance		(Note 5)	-	25	-	-	-	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} × V_{CC} × f_{IN} + I_{CC} / 2 (per F/F)

74VHC74

AC OPERATING REQUIREMENTS

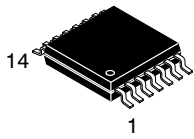
Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = 25°C		T _A = -40°C to +85°C	Unit
			Typ	Guaranteed Minimum		
t _{w(L)} , t _{w(H)}	Minimum Pulse Width (CK)	3.3	–	6.0	7.0	ns
		5.0	–	5.0	5.0	
t _{w(L)}	Minimum Pulse Width (CLR, PR)	3.3	–	6.0	7.0	ns
		5.0	–	5.0	5.0	ns
t _S	Minimum Setup Time	3.3	–	6.0	7.0	ns
		5.0	–	5.0	5.0	
t _H	Minimum Hold Time	3.3	–	0.5	0.5	ns
		5.0	–	0.5	0.5	
t _{REC}	Minimum Recovery Time (CLR, PR)	3.3	–	5.0	5.0	ns
		5.0	–	3.0	3.0	ns

6. V_{CC} is 3.3 ±0.3 V or 5.0 ±0.5 V

ORDERING INFORMATION

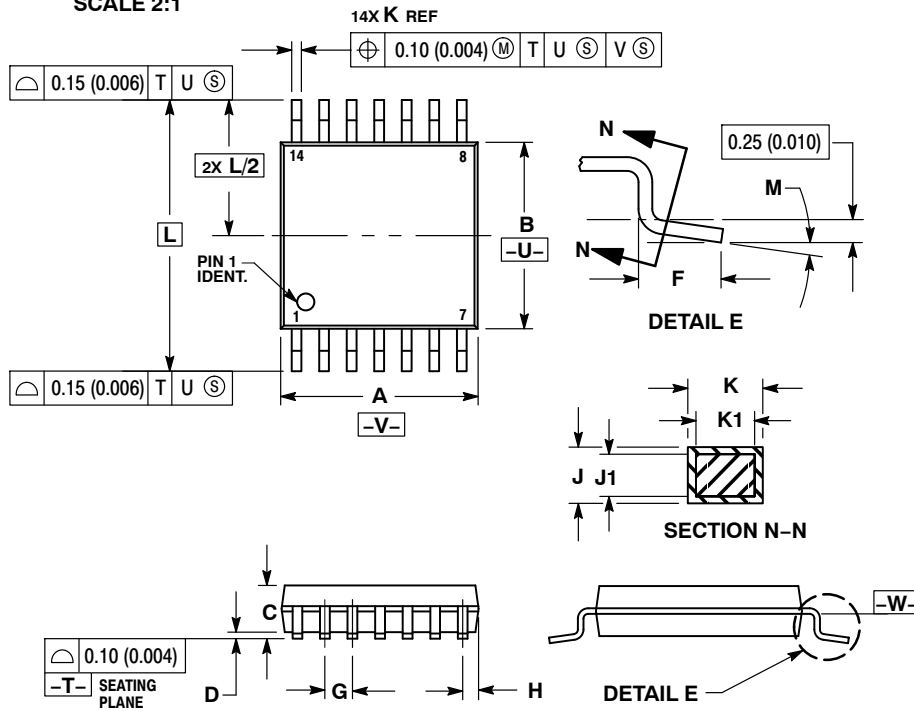
Device Order Number	Top Marking	Package Type	Shipping [†]
74VHC74MTCX	VHC 74	TSSOP-14 WB (Pb-Free, Halide Free)	2,500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TSSOP-14 WB
CASE 948G
ISSUE C

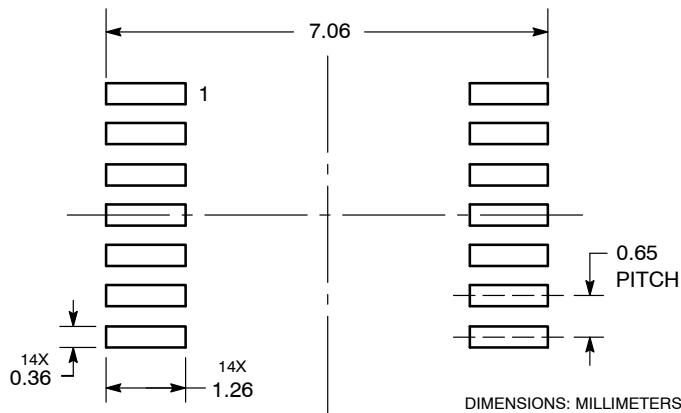
DATE 17 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

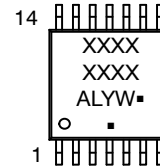
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70246A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-14 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales